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EXAMINER	
MAI,A	
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022850
OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON VA 22202

MMC1/0718

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/358,388	UMEZAWA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-11 and 14-53* is/are pending in the application.

4a) Of the above claim(s) *16-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11,14,15 and 24-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/751,438* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Response to Amendment

1. The amendment filed June 13, 2001 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claims 28 and 29: "depositing oxide film **directly** on the thin thermal oxidation films".

Claims 30-33 and 46: "wherein said oxide films are deposited or buried in the grooves so as *not to include any nitride film* in the grooves".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 28, 29, 30-33 and 46 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "oxide films are deposited or buried in the grooves so as ***not to include any nitride film*** in the grooves" (claims

30-33 and 46) or "depositing oxide film **directly** on the thin thermal oxidation films" (claims 28 and 29) in the application as filed.

Since the limitation of claims 30-33 and 46 fails to get support from the original written specification, therefore, the rejection on merit of the claims are not warranted.

Further, the specification on page 19, line 26, clearly shows that a "Si_3N_4 film may be grown".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9-11, 14, 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. (U.S. Patent No. 4,571,819) in view of Lee et al. (U.S. Patent No. 4,952,524).

Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (19) in the grooves by a CVD method;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the

active areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) annealing the oxide films (19) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using organic silicon based for the CVD oxide film (19).

However, Lee teaches organic silicon based such as BTEOS, PTEOS or BPTEOS are well known in the art to be used for the doped glass.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the oxide film (19) of Rogers using organic silicon based material as taught by Lee because organic silicon based is less toxic and easy to handle.

Furthermore, since the annealing temperature of Rogers is within the claimed range, therefore, the dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$.

With respect to claim 10, the deposition method of Rogers includes one of the methods as claimed.

With respect to claim 11, the ambient during the anneal of Rogers includes nitrogen gas.

With respect to claim 14, trench (13) of Rogers appears to have a depth (d) to width (l) ratio of less than 10.

With respect to claims 15 and 24, the arrangement of the grooves on the semiconductor substrate is clearly a design choice. The method of forming the STI is disclosed.

4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 in view of Lee '524.

Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (19) in the grooves by a CVD method;

(c) annealing the oxide films (19) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using organic silicon based for the CVD oxide film (19).

However, Lee teaches organic silicon based such as BTEOS, PTEOS or BPTEOS are well known in the art to be used for the doped glass.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the oxide film (19) of Rogers using organic silicon based material as taught by Lee because organic silicon based is less toxic and easy to handle.

Furthermore, since the annealing temperature of Rogers is within the claimed range, therefore, the dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$.

5. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 in view of Lee '524.

Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) burying oxide films (19) in the grooves by a CVD method;

(c) annealing the oxide films at a substrate temperature of which is greater than or equal to 1150 °C but less than 1350 °C. (See Figs. 2-8).

Since The annealing temperature of Rogers is within the claimed range, therefore, the limitation of "higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates" as well as "Raman intensity

corresponding to respective ring structures" and "an etching rate by ammonium fluoride solution of the oxide film less than 130 nm/min" are inherent result the *annealing of the substrate at high temperature*.

6. Claims 28 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 in view of Lee '524.

As best understood by examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) forming a thin thermal oxidation film (16) on the inner wall of the grooves;

(c) depositing oxide films (19) on the thin thermal oxidation film by a CVD method;

(d) removing upper parts of the oxide films (19) so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as top surface of a corresponding device region; and

(e) annealing the oxide films at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using organic silicon based for the CVD oxide film (19).

However, Lee teaches organic silicon based such as BTEOS, PTEOS or BPTEOS are well known in the art to be used for the doped glass.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the oxide film (19) of Rogers using organic silicon based material as taught by Lee because organic silicon based is less toxic and easy to handle.

Furthermore, since the annealing temperature of Rogers is within the claimed range, therefore, the dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$.

With respect to claim 34, the thin thermal oxidation films (16) of Rogers are formed by thermal oxidizing inner walls of the grooves (13).

7. Claims 29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 in view of Lee '524.

As best understood by examiner, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) forming thin thermal oxidation films (16) on the inner walls of the grooves;

(c) depositing oxide films (19) on the grooves by a CVD method;

(c) annealing the oxide films (19) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using organic silicon based for the CVD oxide film (19).

However, Lee teaches organic silicon based such as BTEOS, PTEOS or BPTEOS are well known in the art to be used for the doped glass.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the oxide film (19) of Rogers using organic silicon based material as taught by Lee because organic silicon based is less toxic and easy to handle.

Furthermore, since the annealing temperature of Rogers is within the claimed range, therefore, the dislocation density generated in the corresponding device region in a vicinity of the grooves is less than $1/\mu m^2$.

With respect to claim 35, the thin thermal oxidation films (16) of Rogers are formed by thermal oxidizing inner walls of the grooves (13).

8. Claims 36-45 and 49-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 in view of Lee '524.

Rogers teaches a method for forming a microelectronic structure substantially as claimed including:

(a) forming a mask layer (11) on a substrate (10) wherein the mask layer exposed a part (12) of the substrate;

(b) forming a groove (13) in the exposed part of the substrate;

(c) depositing a layer of an insulating film (19) so as to fill the groove and cover the substrate;

(d) annealing the insulating film at a temperature which is greater than or equal to 1150 °C but less than 1350 °C. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly forming a substrate mask layer underlying the photoresist mask (11).

However, Lee teaches that forming a mask layer (15) underlying the photoresist mask (17) to protect the substrate (11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the mask layer (11) of Rogers including an etch mask (15) as taught by Lee to protect the surface of the substrate from the plasma.

With respect to claims 37 and 38, the annealing period of Rogers includes the claimed period.

With respect to claims 39 and 40, the annealing of Rogers is performed in an inert atmosphere (N_2).

With respect to claim 41, the method of Rogers further includes planarizing the insulating film (19) so that the substrate is exposed.

With respect to claim 42, the planarizing of Rogers comprises using CDE method.

With respect to claim 43, the forming the mask layer of Lee comprises forming an oxide layer (13) on the substrate.

With respect to claim 44, forming the layer of the insulating film (19) of Rogers comprises forming an oxide layer (16) on inner walls of the groove (13) and depositing an insulating material (19) on the oxide layer (16) to fill the groove.

With respect to claim 45, the depositing of insulating material (19) of Rogers comprises forming an oxide by CVD.

With respect to claim 49, the depositing of the insulating film (19) of Rogers appears to deposit the insulating film at a thickness larger than a half of the width of the groove.

With respect to claim 50, the forming the mask of Rogers is configured to provide a plurality of grooves at a cross sectional view so as to define a SDG region between a couple of the grooves at the cross sectional view.

With respect to claim 51, Rogers teach all of the features of the claim with the exception of explicitly disclose the width of the SDG between the couple of the grooves (13).

However, the SDG region having a width as claimed does not appears to be critical.

Therefore, given the teaching of the references, it would have been obvious matter of design choice to form the SDG region having a width as claimed, since such a modification would have involved a mere change in the size of the SDG regions. A change in size is generally recognized as being within the level of ordinary skill in the art. See *In re Rose, 105 USPQ 237 (CCPA 1955).*

With respect to claim 52, the method of Rogers further includes forming source/drain regions (36/37) in the SDG region sandwiched by the grooves (13).

With respect to claim 53, the grooves of Rogers appears to have an aspect ratio of less than 10.

9. Claims 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers '819 and Lee '524 as applied to claim 36 above, and further in view of Hunter et al. (U.S. Patent No. 4,631,803).

With respect to claim 48, Rogers and Lee teach all of the features of the claim with the exception of forming groove (13) having taper shape.

However, Hunter teaches forming taper groove (36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form groove (13) of Rogers having taper profile as taught by Hunter to provide sufficient dielectric width for effective isolation.

With respect to claim 47, the groove (36) of Hunter having the width includes the claimed range. However, given the teaching of the references, it would have been obvious matter of design choice to form the groove having a width as claimed, since such a modification would have involved a mere change in the size of the groove. A change in size is generally recognized as being within the level of ordinary skill in the art. See *In re Rose, 105 USPQ 237 (CCPA 1955).*

Response to Arguments

10. Applicant's arguments with respect to claims 9 and 25-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
July 7, 2001

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER